REDUCTION OF ZERO SEQUENCE VOLTAGE USING MULTILEVEL INVERTER FED OPEN-END WINDING INDUCTION MOTOR DRIVE

Mahamkali RANJIT, Sara GOWTAMI, Bommasani GANESH BABU
Department of Electrical and Electronics Engineering, VNR Vignana Jyothi Institute of Engineering and Technology, Hyderabad, Telangana, India, E-mail: ranjit221@gmail.com, gowthami.a699@gmail.com, ganeshbabu_b@vnrvjiet.in

ABSTRACT

Modern inverters have been employed to achieve high dynamic operation in the context of variable speed drives. But due to high $dv/dt$ introduces Zero Sequence Voltage (ZSV) results in adverse effects like bearing currents and electromagnetic interference. In this proposed work, the techniques to overcome the drawbacks due to conventional inverter and multilevel inverter have been presented i.e, by using multilevel inverter fed open end winding. In this paper the performance characteristics of Induction motor with different PWM techniques like sinusoidal PWM (SPWM), third harmonic injection PWM (THIPWM) have been analyzed and the harmonic analysis has been carried out using MATLAB/SIMULINK environment and to validate the proposed work, several simulation results for different modulation index are listed out.

Keywords: Zero Sequence Voltage (ZSV), bearing currents, open end winding induction motor drive, SPWM, THIPWM, modulation index

1. INTRODUCTION

An inverter is a power electronic device used to convert constant DC power to adjustable voltage adjustable frequency AC power drives. To raise the blocking capacity in conventional two-level inverter the switching devices are connected in series. The simultaneous switching of series connected fast devices generates voltage with a high $dv/dt$ at the output terminal of the inverter [1-2]. Due to this the conventional inverter are known to generate “Zero Sequence voltage” or “common mode voltage” because of parasitic stray capacitors inevitably exists inside the AC motor as shown in the Fig. 1. They also result in leakage currents which act as sources of conductive electromagnetic interference in the drive system and also lead to permanent failure in motor bearings.

Fig. 1 Paths of bearing currents inside the motor

In order to eliminate the zero sequence voltage in the context of variable speed motor drives different techniques have been employed and are classified as [3][4][5]:
A) Using isolation transformer, zero sequence impedance, filters,
B) using multilevel inverters, using dual bridge inverter fed induction motor drive(open end winding) or
C) using different modulation techniques like sinusoidal PWM (SPWM), third harmonic injection PWM (THIPWM) and Space vector PWM (SVPWM) techniques [7].

The methods proposed in [A] above increases the system cost as it employs some extra hardware circuitry and complexity in control.

Multilevel inverters are also employed and are extensively used in high power, high-voltage variable speed drive systems. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases due to which low total harmonic distortion (THD) with high efficiency and power factor is obtained [4]. But the complexity, number switches increases as the number of level increases in order to overcome this, this paper is mainly focused on by using proposed inverter fed open end winding (3,4,5,6 level) operated with different control strategies like SPWM, Third harmonic injection control techniques [8][9][10].

The advantages of dual-inverter fed induction motor drive topologies are that the voltage amplitude required to produce air-gap flux in the machine is divided among the two inverters. Therefore, the device ratings as well as $dv/dt$ stress are reduced, which is very important for high power applications and reduces the zero sequence voltage up to great extent and also reduces bearing currents.

2. MULTILEVEL INVERTERS FED OPEN END WINDING INDUCTION MOTOR DRIVE

3&4-level inverter

In this configuration Induction Motor is fed by two inverters from either side which are operated by isolated power supply. A schematic diagram of dual inverter fed Induction Motor drive is shown in the Fig. 2.
From the Fig. 2, INV1 and INV2 are conventional two level inverters. Here S1, S2, S3, S4, S5, S6 are the switches of inverter-1 and S1', S2', S3', S4', S5', S6' are the switches of inverter-2. These two inverters are supplied with the isolated DC-link voltages, these isolated DC-link voltages (i.e. VS1=2VDC/3 & VS2=VDC/3) then the configuration resembles to that of a three level inverter. If the inverters are supplied with the isolated DC-link voltages equal (i.e. VS1=VDC/2 & VS2=VDC/2) then the configuration resembles to that of a three level inverter.

For the given input of VDC/2, these two inverters can attain two levels namely +VDC/2, 0, -VDC/2, here phase A is taken as an example. For voltage level ‘+VDC/2’, S1 and S2 switches are turned on; for ‘0’ voltage level, the switches S2 and S1’ are turned on and for voltage level ‘-VDC/2’, S1’ and S2’ switches are turned on. The switches S1 and S1’, S2 and S2’ are complementary.

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{Pole Voltage (}\text{V}_{\text{AO}}\text{)} & \text{S1} & \text{S2} & \text{S1’} & \text{S2’} \\
\hline
\text{V}_{\text{DC}}/2 & \text{ON} & \text{ON} & \text{OFF} & \text{OFF} \\
0 & \text{OFF} & \text{ON} & \text{ON} & \text{OFF} \\
-\text{V}_{\text{DC}}/2 & \text{OFF} & \text{OFF} & \text{ON} & \text{ON} \\
\hline
\end{array}
\]

**Configuration-I**

5&6-level inverter

In this configuration Induction Motor is fed by two inverters from either side which are operated by isolated power supply, Where INV1 is a 3-level diode clamped multilevel inverter and INV2 is a conventional two level inverter. A schematic diagram of proposed inverter fed open end winding Induction Motor drive is shown in the Fig. 4. Here, S1-S12 are the switches of inverter-1 and S1’-S6’ are the switches of inverter-2. These two inverters are supplied with half of DC-link voltage (i.e. VS1 = VS2 = VDC/2) then the configuration resembles to five level inverter. The phase winding can attain five levels namely +VDC/2 (+state), +VDC/4 (+state), 0, -VDC/2 (-state) and -VDC/4 (-state).

The most commonly used topology is diode clamped inverter, in which the diode is used to clamp the dc bus voltage. The diode clamped multilevel inverter uses capacitors connected in series to divide up the dc bus voltage into a set of voltage levels. The topology of diode-clamped (neutral-point clamped) three-level inverter is shown in the below Fig. 3. The circuit has 12 power switching devices and 6 clamped diodes with two pairs of switches and two diodes on each leg. Two capacitors, C1 and C2 are connected in series in such a way that the bus voltage is divided into three-level. The midpoint of the two capacitors can be defined as the neutral point “O” as a result the switch voltage is limited to half the level of the dc-bus voltage VDC/2. Thus, the voltage stress of switching device is greatly reduced. The output voltage VAO i.e. pole voltage has three different states: +VDC/2, 0, -VDC/2. Here phase A is taken as an example. For voltage level ‘+VDC/2’, S1 and S2 switches are turned on; for ‘0’ voltage level, the switches S2 and S1’ are turned on and for voltage level ‘-VDC/2’, S1’ and S2’ switches are turned on. The switches S1 and S1’, S2 and S2’ are complementary.
If the inverters are supplied with isolated DC-link voltage (i.e. $V_{S1}=2V_{DC}/3$ & $V_{S2}=V_{DC}/6$) then the configuration resembles to that of a six level inverter whose working principle is similar to five level inverter. The Zero Sequence voltage or common mode voltage is given by the equation (4). The line voltages is obtained from the equations (5)-(7).

Configuration-II

5&6-level inverter

A schematic diagram of inverter fed open end winding Induction Motor drive is shown in the Fig. 5 Where INV-X is a 3-level inverter and INV-Y is a conventional two level inverter. The three level inverter (i.e. INV-X) is comprised of two, two level inverters (i.e. INV-1 & INV-2) connected in cascaded so that it resembles to that of a three level inverter.

In order to have efficient and better performance of inverter different modulation techniques have been proposed. Multilevel inversion is a power conversion strategy in which the output voltage is obtained in steps thus bringing the output closer to a sine wave and reduces the Total Harmonic Distortion. In Pulse Width Modulation (PWM) for a fixed DC input we get a controlled AC output by adjusting turn on and turn off of device. In this method, it mitigates lower order harmonics. But, more pulses mean more switching losses [7].

Sinusoidal PWM

In this scheme, three sinusoidal reference waves each shifted by 120° are used. A triangular carrier wave is compared with the reference signal corresponding to a phase to generate the gating signals for that phase. At every instant sinusoidal signal at desired frequency is compared with each carrier signal at high frequency. In this comparison if modulating signal is greater than triangular carrier signal, then signal is given to appropriate semi-conductor switch in respective legs. The reference voltages for a three-phase topology for balanced three-phase system are given by:

$$V_{Aref}(t) = V_m \sin(\omega t)$$
$$V_{Bref}(t) = V_m \sin(\omega t - 2\pi/3)$$
$$V_{Cref}(t) = V_m \sin(\omega t - 4\pi/3)$$

Modulation Index = \frac{Amplitude of Reference Signal(Am)}{Amplitude of carrier Signal (Ac)}

In Sinusoidal PWM technique dc bus utilization is poor. To achieve more DC bus utilization to improve the output voltage profile we will go for third harmonic injection PWM and Space Vector PWM techniques.
Third Harmonic Injection PWM

The sinusoidal PWM is unable to fully utilize the DC bus supply voltage and THD is also higher. So, the third harmonic injection pulse width modulation (THIPWM) technique was developed to increase the inverter performance. In this technique, a third harmonic component is superimposed on the fundamental which is given by the following equation

\[ y = \frac{2}{\sqrt{3}}(\sin \omega t + K\sin 3\omega t) \]

Here, \( k=1/6 \) i.e. Injecting one sixth of the third harmonic component to the fundamental component or \( K=1/4 \) i.e. Injecting one fourth of the third harmonic component to the fundamental component.

4. SIMULATION RESULTS

A) For Diode Clamped multilevel inverter (three level) fed I.M drive with SPWM control

A 3-level multilevel inverter (i.e. DCMLI) fed induction motor drive is modeled and is simulated by employing Sinusoidal pulse width modulation (SPWM) control technique with Modulation index = 1(over modulation) and the reference and carrier wave comparison, output phase voltage, line voltage and ZSV of the inverter are shown in Fig. 6.

![Fig. 6 Modulating signal, Pole voltage, Line voltage, ZSV for 3-level inverter Using SPWM](image)

The performance characteristics of Induction motor drive with SPWM controlled 3-Level Inverter (DCMLI) i.e. Stator currents, Torque, Speed shown in the fig. The motor achieves steady state at 0.15 sec and load is applied from 0.5 to 0.8 sec and then reaches its steady state as shown in Fig. 7.

![Fig. 7 Performance characteristics of IM drive with 3-level inverter Under load Condition](image)

For 3-level multilevel inverter I.M drive using SPWM

3-level multilevel inverter fed I.M drive is modeled and is simulated by employing Sinusoidal pulse width modulation (SPWM) control technique with Modulation index = 1(over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 3 level inverter are shown in Fig. 8.

![Fig. 8 Modulating signal, Pole voltage, Line voltage, phase voltage, ZSV for proposed 3-level inverter using SPWM](image)

For 4-level multilevel inverter I.M drive using SPWM

4-level multilevel inverter fed I.M drive is modeled and is simulated by employing Sinusoidal pulse width modulation (SPWM) control technique with Modulation index = 1(over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 4 level inverter are shown in Fig. 9.
Reduction of Zero Sequence Voltage Using Multilevel Inverter Fed Open-End Winding Induction Motor Drive

Configuration-I

For 5-level multilevel inverter fed I.M drive using SPWM

5-level multilevel inverter fed I.M drive is modeled and is simulated by employing Sinusoidal pulse width modulation (SPWM) control technique with Modulation index = 1 (over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 5 level inverter are shown in Fig. 10.

Fig. 10 Modulating signal, Pole voltage, Line voltage, phase voltage, ZSV for proposed 5-level inverter using SPWM

For 6-level multilevel inverter fed I.M drive using SPWM

6-level multilevel inverter fed I.M drive is modeled and is simulated by employing Sinusoidal pulse width modulation (SPWM) control technique with Modulation index = 1 (over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 6 level inverter are shown in Fig. 11.

Fig. 11 Modulating signal, Pole voltage, Line voltage, phase voltage, ZSV for proposed 6-level inverter using SPWM

Configuration-II

For 5-level multilevel inverter fed I.M drive using SPWM technique

5-level multilevel inverter fed I.M drive is modeled and is simulated by employing Sinusoidal pulse width modulation (SPWM) control technique with Modulation index = 1 (over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 5 level inverter are shown in Fig. 12.

Fig. 12 Modulating signal, Pole voltage, Line voltage, phase voltage, ZSV for proposed 5-level inverter using SPWM

For 6-level multilevel inverter fed I.M drive using SPWM technique

6-level multilevel inverter fed I.M drive is modeled and is simulated by employing Sinusoidal pulse width modulation (SPWM) control technique with Modulation index = 1 (over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 6 level inverter are shown in Fig. 13.

Fig. 13 Modulating signal, Pole voltage, Line voltage, phase voltage, ZSV for proposed 6-level inverter using SPWM
B) For Diode Clamped multilevel inverter (three level) fed I.M drive with THIPWM control

A 3-level multilevel inverter (i.e. DCMLI) fed induction motor drive is modeled and is simulated by employing Third Harmonic Injection pulse width modulation (THIPWM) control technique with Modulation index = 1 (over modulation) and the reference and carrier wave comparison, output phase voltage, line voltage and ZSV of the inverter are shown in Fig. 14.

The performance characteristics of Induction motor drive with THIPWM controlled 3-Level Inverter (DCMLI) i.e. Stator currents, Torque response, Speed response shown in the fig. The motor achieves steady state at 0.15 sec and load is applied from 0.5 to 0.8 sec and then reaches its steady state as shown in Fig. 15.

For 3-level multilevel inverter fed I.M drive using THIPWM technique

3-level multilevel inverter fed I.M drive is modeled and is simulated by employing Third Harmonic Injection pulse width modulation (THIPWM) control technique with Modulation index = 1 (over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 3 level inverter are shown in Fig. 16.

For 4-level multilevel inverter fed I.M drive using THIPWM technique

4-level multilevel inverter fed I.M drive is modeled and is simulated by employing Third Harmonic Injection pulse width modulation (THIPWM) control technique with Modulation index = 1 (over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 4 level inverter are shown in Fig. 17.
For 5-level multilevel inverter fed I.M drive using THIPWM technique

5-level multilevel inverter fed I.M drive is modeled and is simulated by employing Third Harmonic Injection pulse width modulation (THIPWM) control technique with Modulation index = 1(over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 5 level inverter are shown in Fig. 18.

For 6-level multilevel inverter fed I.M drive using THIPWM technique

6-level multilevel inverter fed I.M drive is modeled and is simulated by employing Third Harmonic Injection pulse width modulation (THIPWM) control technique with Modulation index = 1(over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 6 level inverter are shown in Fig. 19.

For 5-level multilevel inverter fed I.M drive using THIPWM technique

5-level multilevel inverter fed I.M drive is modeled and is simulated by employing Third Harmonic Injection pulse width modulation (THIPWM) control technique with Modulation index = 1(over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 5 level inverter are shown in Fig. 20.

For 6-level multilevel inverter fed I.M drive using THIPWM technique

6-level multilevel inverter fed I.M drive is modeled and is simulated by employing THIPWM control technique with Modulation index = 1(over modulation) and the reference and carrier wave comparison, pole voltage, output phase voltage, line voltage and ZSV for proposed 6 level inverter are shown in Fig. 21.
Fig. 21 Modulating signal, Pole voltage, Line voltage, phase voltage, ZSV for proposed 6-level inverter using THIPWM

C) THD Comparison

Table 1 THD values of line voltages for SPWM Technique

<table>
<thead>
<tr>
<th>Inverter type</th>
<th>THD of inverter voltage ($V_{line}$) in under modulation (M.I=0.75) region (%)</th>
<th>THD of inverter Voltage ($V_{line}$/THD) in over modulation (M.I=1) region (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-level</td>
<td>72.26</td>
<td>38.77</td>
</tr>
<tr>
<td>3-level (DCMLI)</td>
<td>42.71</td>
<td>35</td>
</tr>
<tr>
<td>3-level</td>
<td>72.98</td>
<td>39.17</td>
</tr>
<tr>
<td>4-level</td>
<td>75.35</td>
<td>43.33</td>
</tr>
<tr>
<td>Config-I</td>
<td>5-level</td>
<td>60.37</td>
</tr>
<tr>
<td></td>
<td>6-level</td>
<td>45.41</td>
</tr>
<tr>
<td>Config-II</td>
<td>5-level</td>
<td>51.77</td>
</tr>
<tr>
<td></td>
<td>6-level</td>
<td>45.01</td>
</tr>
</tbody>
</table>

Table 2 THD values of line voltages for THIPWM Technique

<table>
<thead>
<tr>
<th>Inverter type</th>
<th>THD of inverter voltage ($V_{line}$) in under modulation (M.I=0.75) region (%)</th>
<th>THD of inverter Voltage ($V_{line}$/THD) in over modulation (M.I=1) region (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>K=1/4</td>
<td>K=1/6</td>
</tr>
<tr>
<td>2-level</td>
<td>69.85</td>
<td>68.36</td>
</tr>
<tr>
<td>3-level (DCMLI)</td>
<td>40.83</td>
<td>40.09</td>
</tr>
<tr>
<td>3-level</td>
<td>70.43</td>
<td>65.8</td>
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<tr>
<td>4-level</td>
<td>71.68</td>
<td>67.81</td>
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<tr>
<td>Config-I</td>
<td>5-level</td>
<td>53.05</td>
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<tr>
<td></td>
<td>6-level</td>
<td>45.45</td>
</tr>
<tr>
<td>Config-II</td>
<td>5-level</td>
<td>46.13</td>
</tr>
<tr>
<td></td>
<td>6-level</td>
<td>41.39</td>
</tr>
</tbody>
</table>

5. CONCLUSION

In this paper, the implementation of inverter fed open winding I.M drive has been done by using different modulation techniques like SPWM and THIPWM. The Zero Sequence Voltage is also mitigated up to greater extent and there is gradual decrement in THD’s using THIPWM because of maximum utilization of DC bus. This work can be extended by using advanced modulation techniques like SVPWM and Discontinuous PWM techniques.

REFERENCES


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BIOGRAPHIES

Mahamkali Ranjit received B.Tech degree from Nalanda Institute of Engineering and Technology, Guntur, Andhra Pradesh in the year 2006. He received M.Tech degree in power electronics and Industrial drives from JNT University in the year 2011. Currently, he is with VNR Vignana Jyothi Institute of Engineering & Technology, Hyderabad, as an Assistant Professor. His areas of interests are power electronic control of drives.

Sara Gowtami received B.Tech degree from Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, Telangana in the year 2012. She received M.Tech degree in power electronics from JNT University Hyderabad in the year 2016. Her areas of interests are multilevel inverters and drives.

Bommasani Ganesh Babu received B.Tech degree from Swarnadhra Institute of Engineering and Technology, Narsapuram, Andhra Pradesh in the year 2010. He received M.Tech degree in power electronics from JNT University Hyderabad in the year 2012. Currently, he is with VNR Vignana Jyothi Institute of Engineering & Technology, Hyderabad, as an Assistant Professor. His areas of interests are multilevel inverters and renewable energy systems.